NEC
NEC Electronics Inc.

μPD23C256E
32,768 x 8-BIT MASK-PROGRAMMABLE CMOS ROM

Revision 1

Description

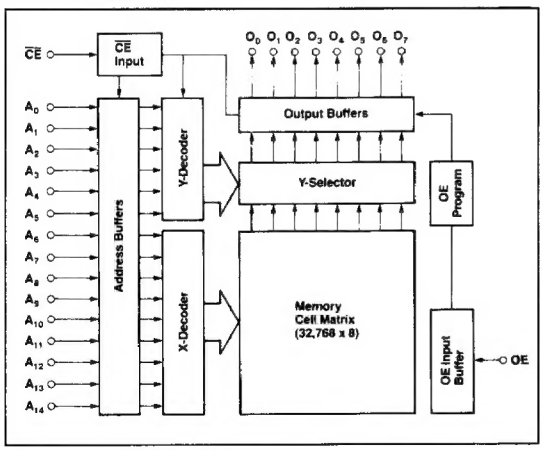
The μPD23C256E is a 262,144-bit Read-only Memory utilizing CMOS silicon gate technology. The device is static in operation, organized as 32,768 words by 8 bits, and has three-state outputs. All inputs and outputs are fully TTL-compatible. The Output Enable pin is mask-programmable and can be specified by selecting 1, 0, or don't-care data. The μPD23C256E is packaged in a 28-pin plastic (μPD23C256EC) DIP and a 28-pin miniflat package (μPD23C256EG). Pinout is compatible with μPD27256 EPROMs.

Features

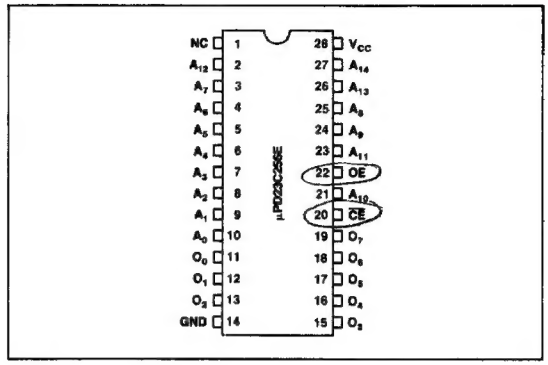
- ☐ 32,768-word by 8-bit organization
- ☐ I/O TTL-compatible
- ☐ Three-state output
- ☐ Single +2.5V to +6.0V power supply
- ☐ Available in plastic DIP and miniflat packages
- ☐ Low power consumption
  - Active: 40mA max
  - Standby: 30μA max
- ☐ 2 performance ranges:

Device	Access Time	Power Supply	
		Active	Standby
μPD23C256E	200ns	25mA	30μA
μPD23C256E-1	150ns	30mA	30μA

Block Diagram



Pin Configuration



Pin Identification

Pin No.	Symbol	Description
1	NC	No Connection
2–10, 21, 23–27	A_0–A_{14}	Address Inputs
11–13, 15–19	O_0–O_7	Data Outputs
14	GND	Ground
20	$\overline{CE}$	Chip Enable
22	OE	Output Enable ①
28	V_{CC}	Single +2.5V to +6.0V Power Supply

Note: ① The active level of the OE input is specified by 0, 1, or x where x equals don't-care data.

10

Absolute Maximum Ratings*

Supply Voltage, V_{CC}	−0.3V to +7V
Input Voltage, V_I	−0.3V to V_{CC} +0.3V
Output Voltage, V_O	−0.3V to V_{CC} +0.3V
Operating Temperature, T_{OPR}	−10°C to +70°C
Storage Temperature, T_{STG}	−65°C to +150°C

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_A = −10°C to +70°C

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Capacitance	C_I			10	pF	f = 1MHz
Output Capacitance	C_O			15	pF	f = 1MHz

DC Characteristics

T_A = −10°C to +70°C; V_{CC} = +5.0V ± 10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input High Voltage	V_{IH}	2.2		V_{CC}+0.3	V	
Input Low Voltage	V_{IL}	−0.3		0.8	V	
Output High Voltage	V_{OH}	2.4			V	I_{OH} = −400μA
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = +3.2mA
Input Leakage Current High	I_{LIH}			10	μA	$V_I = V_{CC}$
Input Leakage Current Low	I_{LIL}			−10	μA	V_I = 0V
Output Leakage Current High	I_{LOH}			10	μA	$V_O = V_{CC}$ (Chip deselected)
Output Leakage Current Low	I_{LOL}			−10	μA	V_O = 0V (Chip deselected)
Power Supply Current	I_{CC1}		14	25	mA	$\overline{CE} = V_{IL}$ μPD23C256E
			17	30	mA	μPD23C256E-1
	I_{CC2}		0.2	1.5	mA	$\overline{CE} = V_{IH}$ (Standby mode)
	I_{CC3}		0.2	30	μA	$\overline{CE} = V_{CC}$ − 0.2V (Standby mode)

DC Characteristics (Cont.)

T_A = −10°C to +70°C; V_{CC} = +2.5V to +6.0V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input High Voltage	V_{IH}	0.7 x V_{CC}		V_{CC} +0.3V	V	
Input Low Voltage	V_{IL}	−0.3		0.55	V	V_{CC} = 2.5V to 4.5V
		−0.3		0.8		V_{CC} = 4.5V to 6.0V
Output High Voltage	V_{OH}	0.75 V_{CC}			V	I_{OH} = −400μA
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = +400μA
Input Leakage Current High	I_{LIH}			10	μA	$V_I = V_{CC}$
Input Leakage Current Low	I_{LIL}			−10	μA	V_I = 0V
Output Leakage Current High	I_{LOH}			10	μA	$V_O = V_{CC}$ (Chip deselected)
Output Leakage Current Low	I_{LOL}			−10	μA	V_O = 0V (Chip deselected)
Power Supply Current	I_{CC1}		3	10	mA	V_{CC} = +3.0V ± 10% μPD23C256E
			6	18	mA	V_{CC} = +5.0V ± 10%
			3.5	10	mA	V_{CC} = +3.0V ± 10% μPD23C256E-1
			7	20	mA	V_{CC} = +5.0V ± 10%
	I_{CC3}		0.1	30	μA	V_{CC} = +3.0V ± 10% $\overline{CE} = V_{DD}$ − 0.2V
			0.2	30	μA	V_{CC} = +5.0V ± 10% (Standby mode)

AC Characteristics

T_A = −10°C to +70°C; V_{CC} = +5.0V ± 10%

Parameter	Symbol	Limits 23C256E Min	Typ	Max	23C256E-1 Min	Typ	Max	Unit	Test Conditions ①
Access Time	t_{ACC}			200			150	ns	
Chip Enable Access Time	t_{CE}			200			150	ns	
Output Enable Access Time	t_{OE}	10		100	10		100	ns	
Output Hold Time	t_{OH}	0			0			ns	
Output Disable Time	t_{DF}	0		90	0		90	ns	②

Notes: ① Input voltage, t_R, t_F = 20ns;
Input and output timing reference levels = 0.8V and 2.0V;
Load = 1TTL + 100pF.
② t_{DF} is specified from $\overline{CE}$ or OE, whichever occurs first.

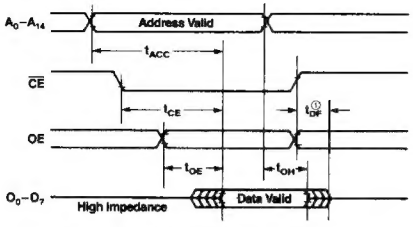
AC Characteristics (Cont.)

T_A = −10°C to +70°C; V_{CC} = +2.5V to +6.0V

Parameter	Symbol	Limits 23C256E Min	Typ	Max	23C256E-1 Min	Typ	Max	Unit	Test Conditions ①
Access Time	t_{ACC}			650			500	ns	
Chip Enable Access Time	t_{CE}			650			500	ns	
Output Enable Access Time	t_{OE}			300			300	ns	
Output Hold Time	t_{OH}	0			0			ns	
Output Disable Time	t_{DF}	0		250	0		250	ns	②

Notes: ① Input and output timing reference levels = V_{IL} and V_{IH};
Load = 150pF.
② t_{DF} is specified from $\overline{CE}$ or OE, whichever occurs first.

Timing Waveform



Note: ① t_{DF} is specified from OE or $\overline{CE}$, whichever occurs first.

Definitions

Access Time, t_{ACC}

Access time is the maximum time between the application of a valid address and the corresponding valid data out.

Chip Enable Access Time, t_{CE}

The maximum time between application of a valid chip enable input and the corresponding valid outputs.

Output Enable Access Time, t_{OE}

The maximum time between application of a valid output enable input and the corresponding valid outputs.

Output Hold Time, t_{OH}

Output hold time is the minimum time after an address change that the previous data remains valid.

Output Disable Time, t_{DF}

Output disable time is the delay between chip selects becoming false and output stages going to the high-impedance state. t_{DF} is specified from $\overline{CE}$ or OE, whichever occurs first.